AMENDMENT TO THE DRAWING

Please amend the drawing by replacing the current drawing sheet 2 with the attached replacement drawing sheet 2.

REMARKS

Claims 1-9, 11-19, 21-36, 38-44, 46-52, 54-59 and 61-78 are pending in the application. Claims 1, 11, 12, 21, 22, 30, 31, 32, 39, 40, 47, 48, 54, 55 and 73 have been amended. Claim 78 is newly added. Reconsideration of this application is respectfully requested.

The Office Action has objected to the drawing because Yes and No legends should be placed adjacent the decision boxes 210d and 220 in Fig. 2. The drawing has been so amended subject to the approval of the Examiner. Therefore, it is submitted that the objection to the drawing is obviated.

The Office Action objects to claim 73 on the ground that "said design specific cell is at least one" should be changed to "the program instructions generate at least one design specific cell". Claim 73 has been so amended.

The Office Action objects to claim 75 on the ground that its base claim 30 references a design-specific cell that is generated using program instructions. This objection is mistaken since claim 75 is dependent on claim 39.

For the reasons set forth above, it is submitted that the objection to claim 73 is obviated by the amendment and the objection to claim 75 is mistaken and, therefore, that the objections should be withdrawn.

The Office Action rejects claims 2, 12, 22, 32, 40, 48, 55 and 62 under U.S.C. 112 as indefinite because the clause "wherein generating comprises evaluating said design-specific cell based on a context of use" is inaccurate and confusing. Although Applicants disagree with this rejection, these claims have been amended in the manner suggested by the Examiner in order to advance the prosecution of this application. Accordingly, it is submitted that the rejection of

claims 2, 12, 22, 32, 40, 48, 55 and 62 under the second paragraph of 35 U.S.C. 112 is obviated by the amendment.

The Office Action rejects claims 1-9, 11-19, 21-36, 38-44, 46-52, 54-59 and 61-77 under 35 U.S.C. 102(e) as anticipated by U.S. Patent No. 6,301,692 to Kumashiro et al., hereafter Kumashiro.

This rejection is inapplicable to the claims as amended because Kumashiro lacks one or more steps or elements of the claims as discussed below.

Kumashiro lacks describing or a description of an integrated circuit (IC) design that includes "at least one design objective of said IC design", as recited in independent claims 1, 21, 30, 31, 39, 47 and 54. The Examiner cites column 3, lines 60-64, as supporting her contention that Kumashiro discloses a describing or description as claimed. However, this citation merely lists objectives that the method is capable of handling, but does not disclose or teach that these objectives are a part of the description of the IC design that is partitioned into "at least one functional block". Moreover, Kumashiro does not disclose or teach that the gate level net list 101 contains any design objective of the logic circuit that is partitioned by circuit dividing processing 102. Therefore, Kumashiro lacks describing or a description of an integrated circuit (IC) design that includes "at least one design objective of said IC design", as recited in independent claims 1, 21, 30, 31, 39, 47 and 54.

Kumashiro also lacks the generating step or generator as recited in independent claims 1, 21, 30, 31, 39, 47 and 54, which have been amended to recite that the "design-specific cell is generated, characterized and optimized at the transistor level based on said design objective". These amended claims now recite that the design-specific cell is "optimized at the transistor level". In

contrast, Kumashiro only optimizes for time delays at the layout level, using the functions of boxes 111, 112, 113, 114 and 115.

Furthermore, Kumashiro clearly is not dealing with design-specific cells, but rather is selecting standard designs or assemblies of standard designs from a library. That is, Kumashiro chooses predefined blocks and then manipulates the layouts of the blocks. In contrast, independent claims 1, 21, 30, 31, 39, 47 and 54 recite a method system or program that generates, characterizes and optimizes a design-specific circuit at the transistor level based on a design objective that is included in a description of the IC design.

With respect to claims 6-9, 16-19, 26-29, 31-36, 38-44, 46-52, 54-59, 61 and 74-77, Kumashiro does not disclose or teach both optimizing the design-specific cell at the transistor level and optimizing the IC design as recited in these claims.

For the reason set forth above, it is submitted that the rejection of claims 1-9, 11-19, 21-36, 38-44, 46-52, 54-59 and 61-7 under 35 U.S.C. 102(e) as anticipated by Kumashiro is obviated by the amendment and should be withdrawn.

The Office Action cites a patent that was not applied in the rejection of the claims. This patent has been reviewed, but is believed to be inapplicable to the claims.

Newly presented claim 78 recites a Markush group for the optimization of the design-specific cell of claim 1. Performance, area and power consumption find support at page 26, line 27 to page 28, line 1, and testability and fault tolerance find support at page 12, lines 6-9, of the specification. Since new claim 78 is dependent on claim 1, it is submitted that claim 78 distinguishes from the

cited art for the same reasons set forth in the discussion of claim 1 above and is, therefore, also allowable.

It is respectfully requested for the reasons set forth above that the objections to the drawing and to the claims be withdrawn, that the rejections under 35 U.S.C. 112 and 35 U.S.C. 102(e) withdrawn, that claims 1-9, 11-19, 21-36, 38-44, 46-52, 54-59 and 61-78 be allowed and that this application be passed to issue.

Respectfully Submitted,

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